

Customer No.: 31561  
Application No.: 10/604,128  
Docket NO.: 10688-US-PA

### **REMARKS**

#### **Present Status of the Application**

The Office Action rejected Claims 1-13 under 35 USC 102(b) as being anticipated by Morita (US 2002/0190974 A1).

After traversing of the aforementioned rejections, Claims 1-13 remain pending in the present application.

#### **Discussion of the claim rejection under 35 USC 102**

*The Office Action has rejected Claims 1-13 under 35 U.S.C. 102(b) as being anticipated by Morita (US-2002/0190974A1, hereinafter "Morita").*

Applicants respectfully traverse the above rejections as set forth below.

Claim 1 of the present invention includes the following feature: **"and an inverter, coupled to the data controller to receive the gray-level signal and to invert the gray-level signal, so as to output a color output signal to the display"**, which is NOT found in Morita. The inverter 182<sub>0-1</sub> found in FIG. 26 in Morita, as cited by the Examiner in the Office Action, for VG<sub>0-1</sub> is NOT used for the same element and NOT used for the same function as the inverter 206 found in the present invention. Therefore, the inverter in Morita is not used in the manner claimed as the inverter of the present invention, thus no anticipation is found. The inverter 182<sub>0-1</sub> found in FIG. 26 in Morita is used as a part of the VG<sub>0-1</sub>, which is found in FIG. 16 in Morita as a part of the signal line drive circuit 40<sub>0</sub>. On the other hand, the inverter 206 in the present invention is used by itself to accomplish

Customer No.: 31561  
Application No.: 10/604,128  
Docket NO.: 10688-US-PA

similar purpose as the DAC shown in FIGs 13A, 13B, and 13C in Morita but at much less power consumption and NOT of the same purpose as the signal line drive circuit 400. As described in paragraphs [0006] & [0025], the present invention "...uses the inverter to output the color output signal to the display .....As the invention does not require use of .... digital to analog converter, which consume a large amount of power, it can achieve the object of saving power." and "... replaces the digital to analog converter 108 with the inverter." On the other hand, Morita clearly uses the digital analog converter instead of a inverter as described in FIG 2 (DAC 38), FIGs 13A, 13B, 13C (DAC 38<sub>A</sub> 38<sub>B</sub> 38<sub>C</sub>), and FIG 16 (DAC<sub>0-1</sub> - DAC<sub>0-24</sub>) in Morita. Therefore, Claim 1 is patentably distinguished over Morita.

Furthermore, with regards to Claims 1 & 6 in the present invention, an implicit feature, that is not explicitly stated but is implied nevertheless, is that NO memory element is required for the driving circuit for a display. The aforementioned is fully supported in paragraph [0026]: "As the invention does not require use of the memory...." and in FIG. 2. On the other hand, Morita includes a RAM 64, which is a form of memory, in FIG. 4 as part of the LCD controller 60 as described in paragraph [0164] in Morita. As a result, the aforementioned provides the present invention with another fact that Claims 1 and 6 patentably distinguish from Morita.

In addition, the following feature in Claim 2: "**inverter inverts the gray-level signal according to a voltage level of the gray-level signal**" is NOT found in Morita based on the same reasoning presented above for Claim 1.

Customer No.: 31561  
Application No.: 10/604,128  
Docket NO.: 10688-US-PA

As a result, dependent Claims 2-5 should also be allowed pending the allowance of Claim 1.

Claim 6 of the present invention includes the following feature: **“and inverting the gray-level signal, so as to output a color output signal to the display”**, which is NOT found in Morita. The inverter 182<sub>0-1</sub> in Morita found in FIG. 26, as cited by the Examiner in the Office Action, for VG<sub>0-1</sub> is NOT used for the same element and NOT used for the same function as the inverter 206 found in the present invention. The inverter 182<sub>0-1</sub> found in FIG. 26 in Morita is used as a part of the VG<sub>0-1</sub> which is found in FIG. 16 in Morita as a part of the signal line drive circuit 40<sub>0</sub>. On the other hand, the inverter 206 in the present invention is used by itself to accomplish the similar purpose as the DAC shown in FIGs 13A, 13B, and 13C in Morita but at much less power consumption and NOT of the same purpose as the signal line drive circuit 40<sub>0</sub>. As described in paragraphs [0006] & [0025], the present invention “...uses the inverter to output the color output signal to the display .....As the invention does not require use of .... digital to analog converter, which consume a large amount of power, it can achieve the object of saving power.” and “... replaces the digital to analog converter 108 with the inverter.” On the other hand, Morita clearly uses the digital analog converter instead of a inverter as described in FIG. 2 (DAC 38), FIGs 13A, 13B, 13C (DAC 38<sub>A</sub> 38<sub>B</sub> 38<sub>C</sub> ), and FIG. 16 (DAC<sub>0-1</sub> - DAC<sub>0-24</sub>) in Morita. And since it is the inverter in the manner claimed that DOES the “inverting” in the claim feature **“and inverting the gray-level signal, so as to output a color output signal to the display”**, as a result, Claim 6 is patentably distinguished over Morita.

Customer No.: 31561  
Application No.: 10/604,128  
Docket NO.: 10688-US-PA

In addition, Claim 8 of the present invention includes the following feature: **“the gray-level signal is inverted by an inverter in the driving circuit.”** This feature in the manner claimed is not found in Morita based on the same reasoning presented in Claims 1 & 6 above with respect to “is inverted” and “an inverter”. As a result, Claim 8 further patentably distinguish over Morita.

Claim 9 of the present invention includes the following feature: **“inverter inverts the gray-level signal according to a voltage level of the gray-level signal”**. Once again, the “inverter” in the manner claimed is not taught in Morita. Therefore, Claim 9 further patentably distinguish over Morita.

Based on the aforementioned arguments, dependent Claims 7-13 should also be allowed pending the allowance of Claim 6.

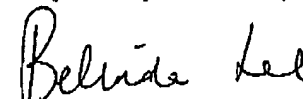
Customer No.: 31561  
Application No.: 10/604,128  
Docket NO.: 10688-US-PA

**CONCLUSION**

For at least the foregoing reasons, it is believed that all the pending Claims 1-13 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

  
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